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REMARKS

The present Amendment is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Applicant asserts that the present invention is new, non-obvious and useful. Favorable reconsideration and allowance of the application are respectfully requested.

Status of Claims

Claims 1-11 and 16-18 are pending in the application.

Claims 12-15 are canceled without prejudice or disclaimer to resubmission in a divisional or continuation application

CLAIM REJECTIONS

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 1-18 under 35 U.S.C. § 103(a), as being unpatentable over Lee et al. (Integrated Parallel Scrambler Design for High-Speed Transmission Systems). Specifically, the Examiner contended that Lee et al. describes a data scrambler to store scrambling values of an m-sequence formed into at least two overlapping swaths of N columns, wherein each swath stores said m-sequence and said m-sequence of one swath is shifted from said m-sequence of a second swath; and a selector adapted to read a current swath N bits at a time for use in scrambling N bits of input in parallel and to shift to the next swath. The Examiner stated that Lee et al. fails to teach a table to store the scrambling values. However, the Examiner contended that it is well known in the art to have a table as an effective storage data structure. The Examiner further contended that the features recited in claims 2-18 are well known in the art for the effective programming of scrambling.

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Applicant respectfully traverses the rejection of claims 1-11 and 16-18, under 35 U.S.C. § 103(a), because a *prima facie* case of obviousness has not been established. Specifically, according to M.P.E.P. §2142, In order to establish a *prima facie* case of obviousness, the prior art references must teach or suggest all the claim limitations.

Independent claims 1 and 16 of the present application recites, in paraphrase, storing scrambling values of an m-sequence in a table, the table formed into at least two overlapping swaths of N columns, wherein each swath stores the m-sequence and the m-sequence of one swath is shifted from the m-sequence of a second swath; reading a current swath N bits at a time for use in scrambling N bits of input data in parallel; and shifting to the next swath (emphasis added). Applicant respectfully submits that Lee et al. does not disclose, teach or suggest at least this feature of claims 1 and 16.

As discussed in detail below, Applicant respectfully traverses the Examiner's contention that Lee et al. discloses storing scrambling values of an m-sequence formed into at least two overlapping swaths of N columns, wherein each swath stores said m-sequence and said m-sequence of one swath is shifted from said m-sequence of a second swath; reading a current swath N bits at a time for use in scrambling N bits of input in parallel; and shifting to the next swath.

Lee et al. describes a parallel scrambling procedure. In particular, section II of Lee et al. describes a mathematical background for performing parallel scrambling. However, Applicant respectfully submits that Lee et al. does not describe, teach or suggest the specific table architecture recited by claims 1 and 16. Therefore, Lee et al., alone or in combination with any other cited references, does not render independent claims 1 and 16 obvious.

Furthermore, section III of Lee et al. describes implementing parallel scrambling using a memory to store a single copy of the m-sequence in a single row; and a pure cycling shift register. Section III of Lee et al. further describes loading the m-sequence to the shift register upon reset, and obtaining tributary m-sequences register tabs spaced from each other by δ tabs. Thus, Lee et al. teaches away from storing scrambling values of an m-sequence in a table formed into at least two overlapping swaths of N columns, wherein each swath stores the m-sequence and the m-sequence of one swath is shifted from the m-sequence of a second swath, because the implementation described by smith stores only a single copy of the m-sequence.

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Independent claim 7 of the present application recites, inter alia, a table having rows and columns adapted to store scrambling values of an m-sequence, wherein a row R has more than N storage elements and stores values of said m-sequence beginning with the (R-1)N+1th value of said m-sequence; and a selector adapted to select N consecutive bits of said m-sequence at a time from said table for use in scrambling N bits of input data (emphasis added). Applicant respectfully submits that Lee et al. does not disclose, teach or suggest this feature of claim 7. Specifically, Applicant respectfully submits that Lee et al. does not disclose, teach or suggest storing the m-sequence in the table architecture recited by claim 7. Furthermore, as discussed above with reference to claims 1 and 16, Lee et al. describes storing a single copy of the m-sequence in a single row, and thus teaches away from the structure recited by claim 7 of the present application.

In view of the above, Applicant respectfully submits that Lee et al., alone or in combination with any other cited references, does not render independent claims 1, 7 and 16 obvious and. Therefore, Applicant respectfully requests that the rejection of claims 1, 7, and 16 under 35 USC §103(a) be withdrawn.

Claims 2-6 depend, directly or indirectly, from independent claim 1 and incorporate all the elements of this claim. Claims 8-11 depend, directly or indirectly, from independent claim 7 and incorporate all the elements of this claim. Claims 17 and 18 depend, directly or indirectly, from independent claim 16 and incorporate all the elements of this claim. Therefore, it is respectfully submitted that claims 2-6, 8-11, and 17-18 are patentable, and thus allowable, at least for the reasons set forth above.

In view of the above, Applicant respectfully requests that the rejection of claims 2-6, 8-11, and 17-18 under 35 USC §103(a) be withdrawn.

Applicant traverses the Examiners contention that all features recited by each one of claims 2-11, and 16-18 are well known in the art for the effective programming of scrambling. Specifically, Applicant traverses the Examiner's contention that the features relating to the table architecture, e.g., as are recited by claims 2-4, 6, 7, 8, 9, 11, 16 and/or 17; and/or the features relating to the configuration of the selector and/or the selection operation, e.g., as are recited by claims 5, 7, 10, 16 and/or 18, are well known in the art. In accordance

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with M.P.E.P. §2144.03, Applicant respectfully requests that the Examiner provide documentary evidence supporting the statement that these features are commonly known.

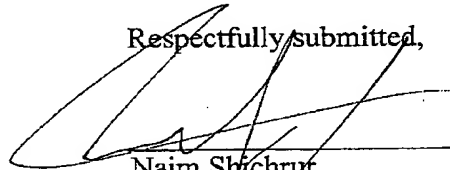
Applicants respectfully submit that in view of the cancellation of claims 12-15, the rejection of claims 12-15 under 35 U.S.C. §103(a) is now moot.

In view of the foregoing remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 50-3355.

Respectfully submitted,



Naim Shichrut
Attorney/Agent for Applicant(s)
Registration No. 56,248

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Pearl Cohen Zedek Latzer, LLP
10 Rockefeller Plaza, Suite 1001
New York, New York 10020
Tel: (212) 632-3480
Fax: (212) 632-3489